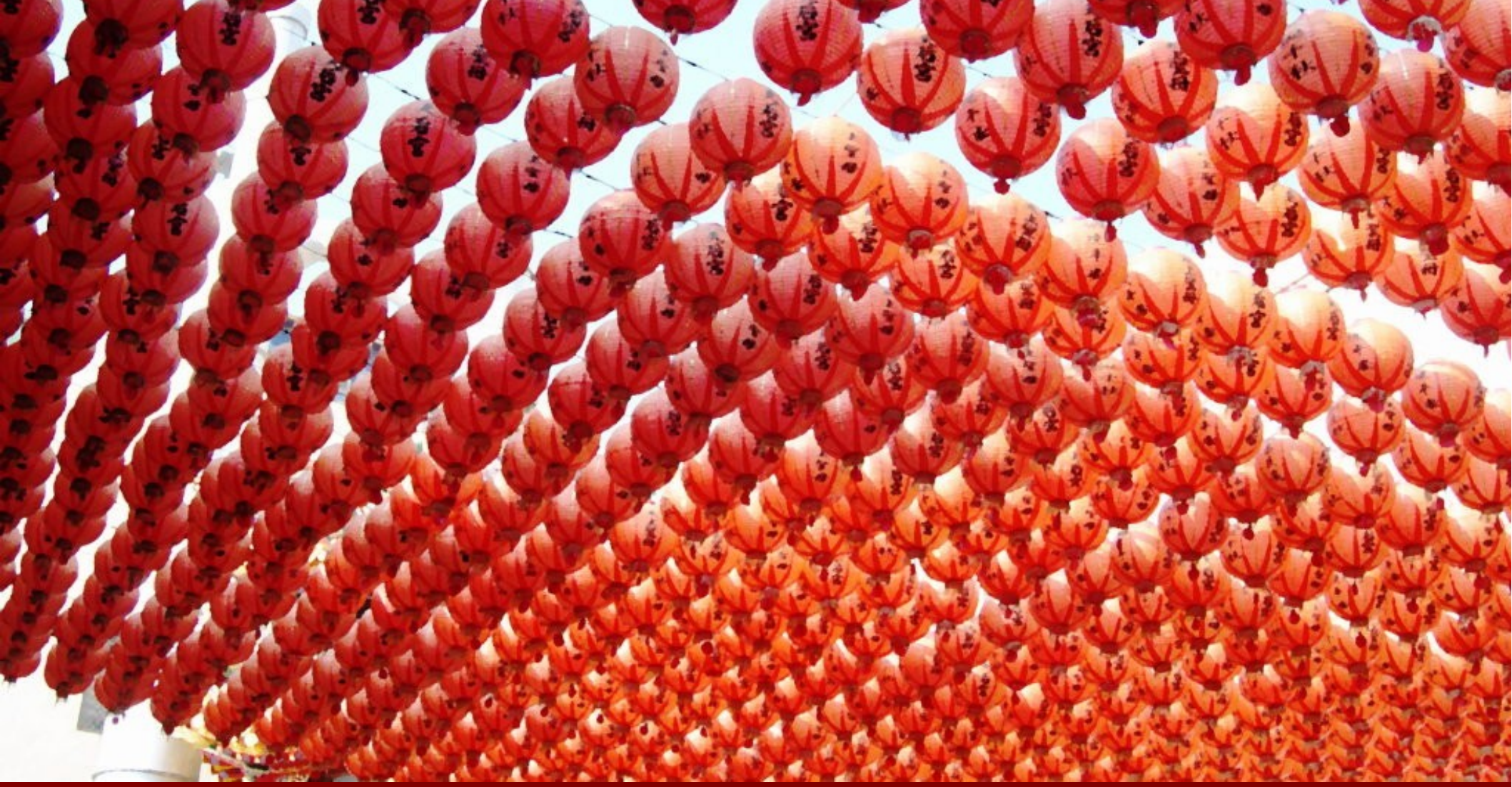

AVR Flash Memory Notes Part One

Exploring the Atmega328P

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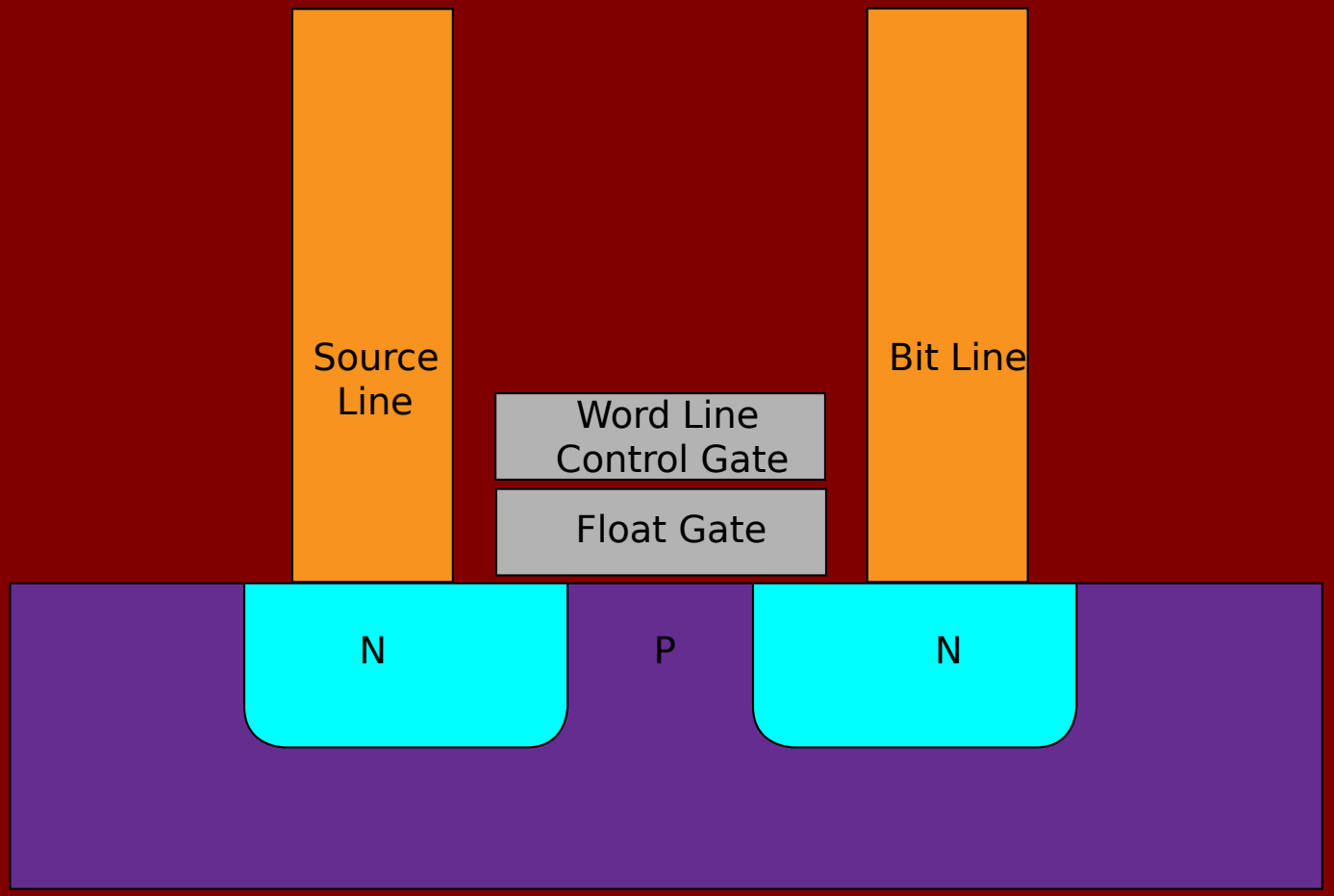
Outline

- Touch on flash operation
- Flash characteristics
- Addressing and access
- Fuses and other special locations
- Unless otherwise noted all specifics are to do with the (Atmel cum Microchip) AVR Atmega328 MPU

Flash Memory Cell (Wikipedia)



Memory Operation

- FET transistor with two gates:
  - Isolated gate that holds a charge
  - Control gate used for access
- Counterintuitive storage:
  - Erased cell without charge is HIGH
  - Cell with charge is LOW
  - So HIGH “bit” is simply “written with nothing” to preserve logic state

Characteristic: Speed

- Read speed of flash inside Atmega328 is “adequate”
  - Supports 50ns read access to avoid “wait states”
- Write speed is slower
- Erase speed is also much slower
- These characteristics hold for other examples of flash and different types, but some varieties have fast write as well as fast read performance
- I’m too lazy to time writes/erases, but maybe for a “part 2” talk

Characteristic: Endurance

- Read endurance until transistor charge is lost. For Atmega328:
  - 1 PPM error over 20 years @ 85C, 100 years at 25C
- Limited erase/write cycles before cells “wear out”
  - “At least 10,000 cycles” for Atmega328 (probably for all AVR family members, but not sure)
- I don’t know about you folks, but I’d CRC-check my flash during POST for a critical app with a long lifespan

Addressing

- Atmega328 flash is composed of 16 bit words
  - Intended application is fetching instructions and AVR instructions are one or more 16 bit words
  - Granularity of read and write access
- Words arranged into 64 word (128 byte) pages
  - This is the erase granularity
- Pages are arranged into two sections: “application” and “bootloader”
  - Size options for bootloader section

More Addressing

- Because read/write access granularity is a 16 bit word, there is no need for byte addresses
- All flash-related addresses with in 328 instructions are WORD ADDRESSES
  - Expressed as byte addresses frequenty to keep us sane
  - But encoded addresses are word addresses
- Nice side effect is that Atmega328 first cousins (e.g. 1284) can access 128KB of flash without muss or fuss

Sections

- Application section is designed to hold you know what
- Bootloader section is designed to hold:
  - Bootloaders (duh)
  - ***ANY CODE TO WRITE TO FLASH***
- ***This means a vanilla application cannot change its own flash memory***
- Common bootloaders do not provide flash write routines usable by application code

Special Regions

- A few special flash memory regions
  - ID signature (MCU type & package)
  - Fuses to set major chip parameters
  - Fuses to control access (“locks”)
- KEY POINT: Some fuses disable access
  - So wrong setting hoses you and forces special “high voltage erase” to recover
- KEY POINT (for me): Default settings frequently preclude application code modifying flash

Brief Outline of Write Operations

- SPM instruction stores words into flash
  - AVR has a Harvard architecture: program and data are in separate address spaces, so regular store won’t work anyway
- Pages can be written a special way:
  - Put data to be written into a special, page-size “temporary buffer” inside the chip (static RAM not ordinarily accessible)
  - Use special form of SPM to copy temp buffer into flash

References

- Wikipedia “flash memory” page: https://en.wikipedia.org/wiki/Flash_memory
- AVR Instruction set: https://en.wikipedia.org/wiki/Atmel_AVR_instruction_set
- Atmega328P datasheet: http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-42735-8-bit-AVR-Microcontroller-ATmega328-328P_Datasheet.pdf

Additional Details

- Following slides not part of planned presentation but provide a bit more detail

Regular Feature Fuses

AVR part name: ATmega328P ▾ Select (141 parts currently listed)

Feature configuration

This allows easy configuration of your AVR device. All changes will be applied instantly.

Features

Int. RC Osc. 8 MHz; Start-up time PWRDWN/RESET: 6 CK/14 CK + 65 ms; [CKSEL=0010 SUT=10]; default value ▾

- ☐ Clock output on PORTB0; [CKOUT=0]
- ☑ Divide clock by 8 internally; [CKDIV8=0]
- ☐ Boot Reset vector Enabled (default address=$0000); [BOOTRST=0]

Boot Flash section size=2048 words Boot start address=$3800; [BOOTSZ=00] ; default value ▾

- ☐ Preserve EEPROM memory through the Chip Erase cycle; [EESAVE=0]
- ☐ Watch-dog Timer always on; [WDTON=0]
- ☑ Serial program downloading (SPI) enabled; [SPIEN=0]
- ☐ Debug Wire enable; [DWEN=0]
- ☐ Reset Disabled (Enable PC6 as i/o pin); [RSTDISBL=0]

Brown-out detection disabled; [BODLEVEL=111] ▾

Apply feature settings

Manual fuse bits configuration

This table allows reviewing and direct editing of the AVR fuse bits. All changes will be applied instantly.

Note: ☐ means unprogrammed (1); ☑ means programmed (0).

Bit	Low	High	Extended
7	☑ **CKDIV8** Divide clock by 8	☐ **RSTDISBL** External reset disable	
6	☐ **CKOUT** Clock output	☐ **DWEN** debugWIRE Enable	
5	☐ **SUT1** Select start-up time	☑ **SPIEN** Enable Serial programming and Data Downloading	
4	☑ **SUT0** Select start-up time	☐ **WDTON** Watchdog Timer Always On	
3	☑ **CKSEL3** Select Clock Source	☐ **EESAVE** EEPROM memory is preserved through chip erase	
2	☑ **CKSEL2** Select Clock Source	☑ **BOOTSZ1** Select boot size	☐ **BODLEVEL2** Brown-out Detector trigger level
1	☐ **CKSEL1** Select Clock Source	☑ **BOOTSZ0** Select boot size	☐ **BODLEVEL1** Brown-out Detector trigger level
0	☑ **CKSEL0** Select Clock Source	☐ **BOOTRST** Select reset vector	☐ **BODLEVEL0** Brown-out Detector trigger level

Special Feature Fuses

28.1 Program And Data Memory Lock Bits

The ATmega 48A/48PA provides two Lock bits and the ATmega88A/88PA/168A/168PA/328/328Pprovides six Lock bits. These can be left unprogrammed (“1”) or can be programmed (“0”) to obtain the additional features listed in Table 28-2. The Lock bits can only be erased to “1” with the Chip Erase command.

The ATmega 48A/48PA has no separate Boot Loader section, and the SPM instruction is enabled for the whole Flash if the SELFPRGEN fuse is programmed (“0”). Otherwise the SPM instruction is disabled.

Table 28-1. Lock Bit Byte[1]

Lock Bit Byte	Bit No	Description	Default Value
	7	–	1 (unprogrammed)
	6	–	1 (unprogrammed)
BLB12[2]	5	Boot Lock bit	1 (unprogrammed)
BLB11[2]	4	Boot Lock bit	1 (unprogrammed)
BLB02[2]	3	Boot Lock bit	1 (unprogrammed)
BLB01[2]	2	Boot Lock bit	1 (unprogrammed)
LB2	1	Lock bit	1 (unprogrammed)
LB1	0	Lock bit	1 (unprogrammed)

Notes: 1. “1” means unprogrammed, “0” means programmed.
2. Only on ATmega88A/88PA/168A/168PA/328/328P.

Table 28-2. Lock Bit Protection Modes[1][2]

Memory Lock Bits			Protection Type
LB Mode	LB2	LB1	
1	1	1	No memory lock features enabled.
2	1	0	Further programming of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Fuse bits are locked in both Serial and Parallel Programming mode.[1]
3	0	0	Further programming and verification of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Boot Lock bits and Fuse bits are locked in both Serial and Parallel Programming mode.[1]

Notes: 1. Program the Fuse bits and Boot Lock bits before programming the LB1 and LB2.
2. “1” means unprogrammed, “0” means programmed

How To Mess Up Your Chip

AVR part name: ATmega328P ▾ Select (141 parts currently listed)

Feature configuration

This allows easy configuration of your AVR device. All changes will be applied instantly.

Features

Int. RC Osc. 8 MHz; Start-up time PWRDWN/RESET: 6 CK/14 CK + 65 ms; [CKSEL=0010 SUT=10]; default value ▾

- ☐ Clock output on PORTB0; [CKOUT=0]
- ☑ Divide clock by 8 internally; [CKDIV8=0]
- ☐ Boot Reset vector Enabled (default address=$0000); [BOOTRST=0]

Boot Flash section size=2048 words Boot start address=$3800; [BOOTSZ=00] ; default value ▾

- ☐ Preserve EEPROM memory through the Chip Erase cycle; [EESAVE=0]
- ☐ Watch-dog Timer always on; [WDTON=0]
- ☑ Serial program downloading (SPI) enabled; [SPIEN=0]
- ☐ Debug Wire enable; [DWEN=0]
- ☐ Reset Disabled (Enable PC6 as i/o pin); [RSTDISBL=0]

Brown-out detection disabled; [BODLEVEL=111] ▾

Apply feature settings

Manual fuse bits configuration

This table allows reviewing and direct editing of the AVR fuse bits. All changes will be applied instantly.

Note: ☐ means unprogrammed (1); ☑ means programmed (0).

Bit	Low	High	Extended
7	☑ **CKDIV8** Divide clock by 8	☐ **RSTDISBL**	
6	☐ **CKOUT** Clock output	☐ **DWEN** debugWIRE Enable	
5	☐ **SUT1** Select start-up time	☑ **SPIEN** Enable Serial Programming and Data Downloading	
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2	☑ **CKSEL2** Select Clock Source	☑ **BOOTSZ1** Select boot size	☐ **BODLEVEL2** Brown-out Detector trigger level
1	☐ **CKSEL1** Select Clock Source	☑ **BOOTSZ0** Select boot size	☐ **BODLEVEL1** Brown-out Detector trigger level
0	☑ **CKSEL0** Select Clock Source	☐ **BOOTRST** Select reset vector	☐ **BODLEVEL0** Brown-out Detector trigger level

Nails In The Coffin

28.1 Program And Data Memory Lock Bits

The ATmega 48A/48PA provides two Lock bits and the ATmega88A/88PA/168A/168PA/328/328Pprovides six Lock bits. These can be left unprogrammed (“1”) or can be programmed (“0”) to obtain the additional features listed in Table 28-2. The Lock bits can only be erased to “1” with the Chip Erase command.

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Table 28-1. Lock Bit Byte(1)

Lock Bit Byte	Bit No	Description	Default Value
	7	–	1 (unprogrammed)
	6	–	1 (unprogrammed)
BLB12(2)	5	Boot Lock bit	1 (unprogrammed)
BLB11(2)	4	Boot Lock bit	1 (unprogrammed)
BLB02(2)	3	Boot Lock bit	1 (unprogrammed)
BLB01(2)	2	Boot Lock bit	1 (unprogrammed)
LB2	1	Lock bit	1 (unprogrammed)
LB1	0	Lock bit	1 (unprogrammed)

Notes: 1. “1” means unprogrammed, “0” means programmed.
2. Only on ATmega88A/88PA/168A/168PA/328/328P.

Table 28-2. Lock Bit Protection Modes(1)(2)

Memory Lock Bits			Protection Type
LB Mode	LB2	LB1	
1	1	1	No memory lock features enabled.
2	1	0	Further programming of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Fuse bits are locked in both Serial and Parallel Programming mode.(1)
3	0	0	Further programming and verification of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Boot Lock bits and Fuse bits are locked in both Serial and Parallel Programming mode.(1)

Notes: 1. Program the Fuse bits and Boot Lock bits before programming the LB1 and LB2.
2. “1” means unprogrammed, “0” means programmed